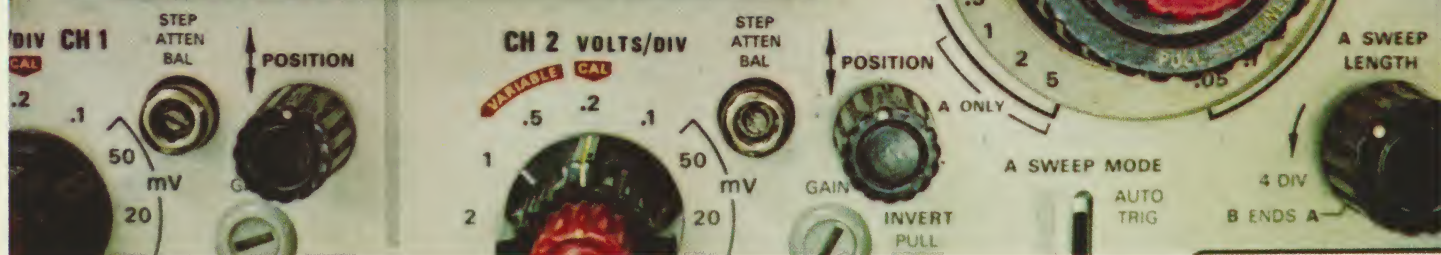


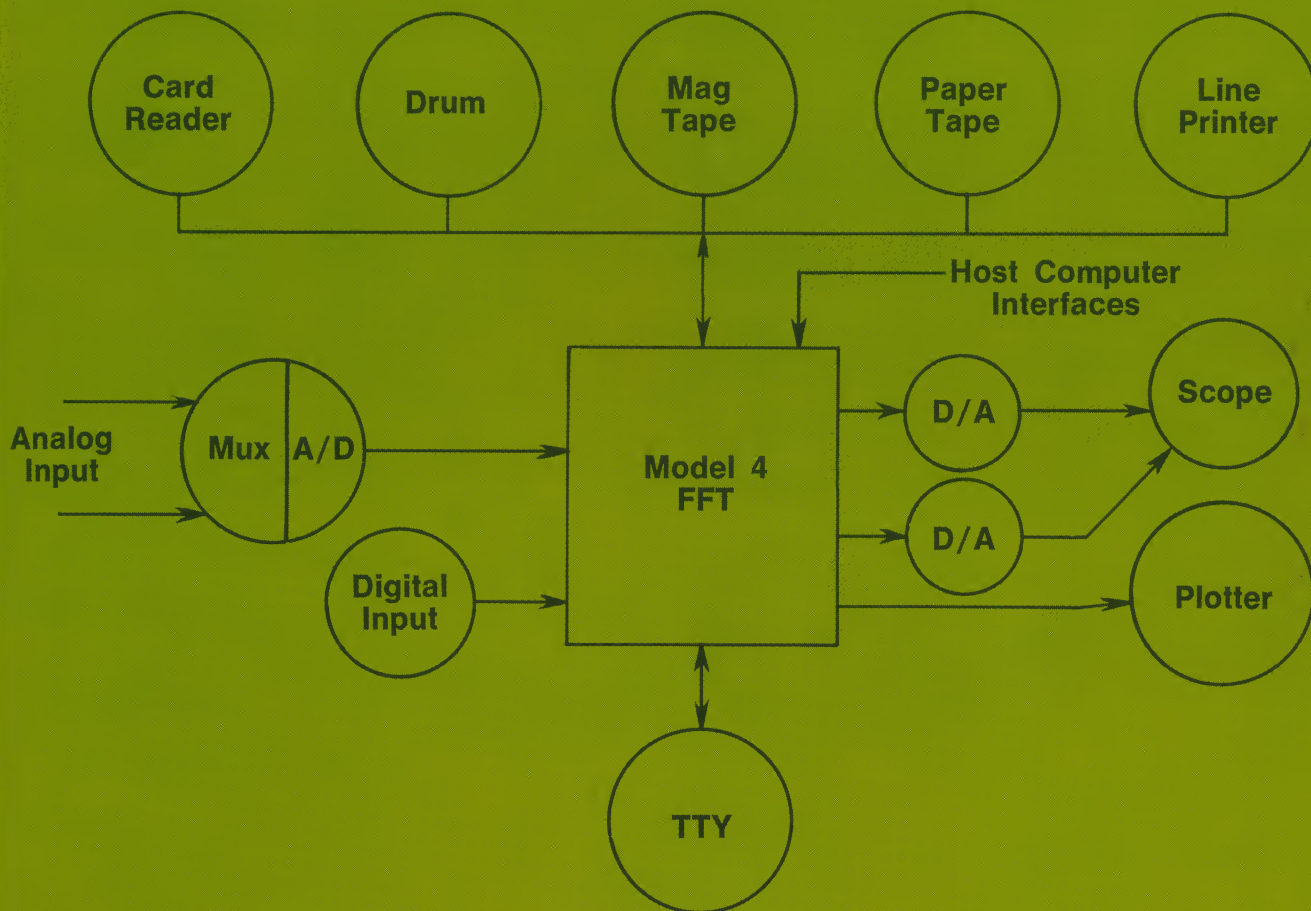
INTERDATA®

$$f(t) = \sum_{k=-\infty}^{\infty} f_k \exp(2\pi i k t / N)$$



Interdata FFT at a glance

- Read-Only Memory plus software routines!
- Most Powerful System available under \$20,000!
- Flexible Option set for high speed analog or digital input!
- Floating Point outputs!
- Designed for host computer interface!
- Minimum Programming knowledge required!
- Performs Direct, Inverse, Convolution . . . Fourier Transforms!
- Complete GP capability independent of FFT processing!



Fast Fourier transforms at half the cost

The reliable INTERDATA Model 4 General Purpose Computer now offers Fast Fourier Transform (FFT) capability as optional FIRMware. The FFT option is a set of Read-Only-Memory (FIRMware) routines integrated with software. It enables the user to compute the discrete Fourier Transform, and its inverse of a maximum of 16 bit data (15 bits + sign), using a version of the Cooley-Tukey algorithm. The INTERDATA FFT will compute transforms for real or complex arrays whose size is a function of 2^m . Up to 1024 complex, or 2048 real

points can be handled with the standard 8K byte memory. Memory sizes over 40K bytes can support a 8,192 complex or 16,384 real point array.

Software + Firmware = speed and efficiency

For real time on-line applications, INTERDATA's Model 4 with FFT option offers you about the ultimate in speed and efficiency. Just look at these examples:

- Through FIRMware a significant increase in speed over conventional software is realized.
- FIRMware eliminates core accesses for instruction fetches. This permits

you simultaneous computation of FFT and direct memory or selector channel use.

- Offers complete general purpose computer capability.
- The maximum non-interruptable time is less than 160 usec during FFT computation.

Of additional significance is the inclusion within a software package of a routine which, utilizing FIRMware, permits computation of FFT for two real arrays simultaneously. This yields a 20% saving in execution time over computing each FFT by itself. It is also useful for convolving two real data sets.

Sine and Cosine Computation

The Read-Only-Memory routines use a look-up table for computation of sine and cosine values. The table is provided as part of the software and resides in core. It has 128 points from 0 to 90 degrees. Interpolation is done for array sizes larger than 512 complex, or 1024 real points. If desired, the user can expand the size of the trig table to accommodate

larger arrays without interpolation or modification of the FFT package.

This allows the user to specify the number of bits of precision (1-16) contained in the input data. The user can also specify a scale factor "n" of the data array where the real value is the array multiplied by 2ⁿ. The FFT routines automatically update the

scale factor for the array as multiplications are done and the final scale factor is returned to the user at the end of the FFT computation.

Typical accuracy to compute the FFT for 512 complex points of 10 bit data (9 bits + sign) is 48 db (.4%), and of 16 bit data (15 bits + sign) is better than 60 db (.1%).

Typical computation times including coefficient reordering				
	10 bit data		16 bit data	
64 Complex Points	24 msec		28 msec	
512 Complex Points	300 msec		343 msec	
	10 bit data		16 bit data	
64 Real Points	one at a time 19 msec	Two at once* 26 msec	one at a time 21 msec	Two at once* 30 msec
512 Real Points	200 msec	300 msec	230 msec	350 msec

* Total for both

Firmware instruction sets

FFT micro-programmed instructions useful for data handling are made available to a FFT/Model 4 user as standard INTERDATA format instructions for use in normal program applications. They are: Load Fullword (32 bits), Store Fullword (32 bits), Variable Precision Logical Multiply and Array Scaling which shifts all array elements left or right arithmetically with rounding.

The FFT is invoked by calling up software routines in the usual INTERDATA format:

BAL		FFT Instructions	
DC	15, 'name'		'name'
DC	A (Array)	Address of ARRAY	RFFT – Real Data FFT
DC	A (M)	Address of M where 2 ^m = No. of array points	IRFFT – Inverse FFT to real array
DC	A (N)	Address of N where 2 ⁿ (Array Data) = Actual Data	CFFT – Complex data FFT
DC	A (Precision)	Address of Precision = No. of bits in data point	ICFFT – Inverse FFT to complex array
			R2FFT – Two real data FFT at once
			IR2FFT – Inverse FFT to two real

Model 4 specifications

Data Word Length — 8, 16, 32 bits
(parity option)

Memory Cycle Time —

1.0 microsecond — Core Memory

400 nanosecond — Read-only-memory

Word Size — 16 bits

General Registers — 16 hardware
registers (16 bits each)

Hardware Index Registers — 15 general
registers may be used for indexing

Basic Memory — 4K bytes, expandable
to 65K bytes

Directly Addressable Memory — 65K bytes

Machine Code — Two's Complement

Instruction Repertoire — over 75 standard
instructions

16 bit—Load Halfword—2.8 microseconds

16 bit—Add Halfword—3.2 microseconds

16 bit—Multiply—3.8 microseconds
(optional)

Input/Output

Program Transfer — 25KBS

Block Transfer — 150 KBS (with high
speed option 4-101)
500 KBS (with selector
channel 7-201)

Interrupts — 2-256 levels
8 levels with arm/disarm
and mask (optional)

Display Panel

Control Switches — Power initialize
execute

Mode Control — Run, halt, single op,
variable speed, address input, memory
location, memory data

Speed Control — Variable, 1 cycle/sec
to 100 cycle/sec

Display — Two registers simultaneously
selectable

Switches — Sixteen data/sense

Mechanical

Size — 10½" x 19" x 4" (rack
mountable)

Power — 325 watts, 115 VAC ± 10%,
47-63 hertz

Weight — 56 lbs.

Temperature:

Operating — 0° to 50°C

Storage — 55° to 85°C

Humidity — 0 to 90% relative

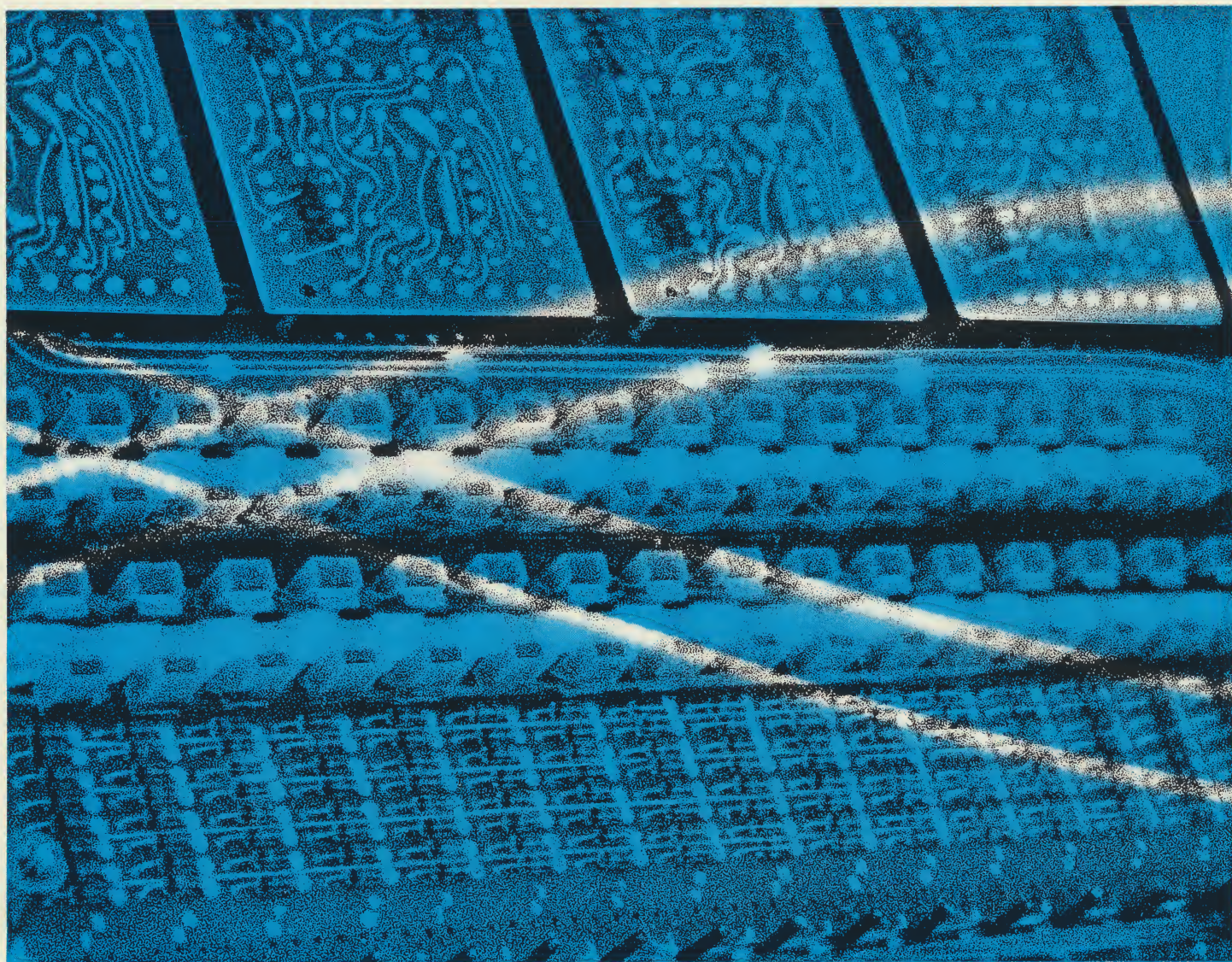
Reliability

MTBF — 6,000 hrs. (Mainframe and
4KB Memory)

In summation

If you're thinking of committing \$50,000 to \$150,000 towards the purchase of a computer to perform Fast Fourier Transforms, then why not buy a "total computer" — the INTERDATA FFT/Model 4. It's available now, and at half the price of what you'd expect to pay for FFT alone.

The FFT/Model 4 was created by INTERDATA, a pioneer in Read-Only-Memory. To perform sophisticated Fast Fourier Transforms demands the best hardware, software and FIRMware obtainable. Others are using the INTERDATA FFT option on their Model 4 — shouldn't you?



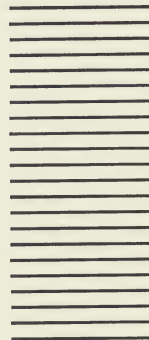
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Yes, I am interested in learning more about the interdata Model 4 FFT.

NAME

STREET

CITY

STATE

ZIP CODE

My application is _____

☐ Have a salesman phone me.

Phone _____

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513-277-1142

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Cupertino, Calif. 95014
408-257-3418

UNITED KINGDOM

Interdata Ltd.
Station House
Harrow Road
Wembley, Middlesex
01-903-2611

General Purpose Systems Price List

PRODUCT NUMBER	DESCRIPTION	UNIT PRICE
3-151	GENERAL PURPOSE PROCESSOR <u>Model 3 System includes:</u> 8K Byte of Core Memory, standard instruction set, hardware multiply and divide, read block and write block, buffered multiplexor channel, priority interrupts for 256 devices, display panel, and power supply. <u>Model 4 System includes:</u> standard instruction set, buffered multiplexor channel, priority interrupts for 256 devices, display panel, and power supply.	\$ 8,900
4-151	<u>Model 4 with 8 KB of Core Memory</u>	10,900
4-155	<u>Model 4 with 32 KB Mass Memory</u>	19,300
4-156	<u>Model 4 with 64 KB Mass Memory</u>	28,900
4-101	PROCESSOR OPTIONS <u>High Speed Arithmetic and Input/Output — Model 4</u> Floating Point Instruction Set Provides hardware floating add, subtract, multiply, divide, compare, load and store. Includes 4-101 (Model 4 only)	750
4-102	<u>Floating Point Instruction Set</u>	1,250
3-111	<u>Power Fail for Model 3</u>	400
4-111	<u>Power Fail for Model 4</u>	400
3-112	<u>Auto-Restart for Power Fail</u> (Requires 3-111)	200
4-112	<u>Auto-Restart for Power Fail</u> (Requires 4-111)	200
7-113	<u>Hard-wired Memory Protect</u>	800
7-114	<u>Programmable Memory Protect</u> (Requires 7-113)	1,500
7-201	HIGH SPEED AUTONOMOUS INPUT/OUTPUT <u>Selector Channel</u> Provides a high speed input/output channel for standard peripheral devices. Data is input/output directly to/from Core Memory at a maximum transfer rate of 500K bytes per second. (Requires 7-203)	2,300
7-203	<u>High Speed Memory Bus Controller</u> Converts the core memory bus to a multi-access bus.	1,200

PRODUCT NUMBER	DESCRIPTION	UNIT PRICE
7-204	HIGH SPEED AUTONOMOUS INPUT/OUTPUT (Cont.) <u>Standard Memory Bus Interface</u> A basic interface to the memory bus (Requires 7-203)	\$ 700
7-314	<u>8,192 Byte Memory Module</u>	4,800
7-317	<u>16,384 Byte Memory Module</u>	9,600
7-318	<u>24,576 Byte Memory Module</u>	14,400
7-319	<u>32,768 Byte Memory Module</u>	19,200
7-115	<u>Parity Option for initial 8,192 Byte Memory Module</u> (one required per 64K Byte Memory System, Modular Memory Only)	1,000
7-116	<u>Parity Option for each additional 8,192 Byte Memory Module</u> (Modular Memory Only)	500
7-117	<u>Parity Option for 32 KB Mass Memory</u>	1,500
7-118	<u>Parity Option for 64 KB Mass Memory</u>	2,000
7-420	PERIPHERAL DEVICES All peripheral devices include necessary interface to the processor. Teletypes and Typewriters <u>ASR Model 33</u>	1,700
7-422	<u>ASR Model 35</u>	4,500
7-424	<u>KSR Model 33</u>	1,600
7-425	<u>KSR Model 35</u>	2,900
7-410	Paper Tape and Card Equipment <u>Paper Tape Reader</u> , Uni-directional 300 cps, Rack Mounting with fanfold bins	2,500
7-411	<u>Paper Tape Reader</u> , Bi-directional, 300 cps, Rack Mounting with fanfold bins	3,200
7-415	<u>Paper Tape Handler</u> with 8" NAB Reels	1,600
7-412	<u>Paper Tape Punch</u> , 60 cps	3,800
7-413	<u>Combination Reader/Punch</u>	5,300
7-510	<u>Card Reader</u> , 200 cpm	4,300
7-550	<u>Line Printer</u> , 300 lpm	21,900
7-445	132 columns, 64 characters <u>X-Y Incremental Plotter</u> : Plots 18,000 steps per minute, .01" or .005" sets 12" wide paper	8,900
7-442	<u>X-Y Oscilloscope Display</u> Plots point to point, 10-bits/axis	3,600

PRODUCT NUMBER	DESCRIPTION	UNIT PRICE
	MAGNETIC STORAGE SYSTEMS IBM Compatible Magnetic Tape 10.5" Reels Standard (All Tape Transports require either 7-201 and 7-203 or 4-101)	
7-607	<u>7 Track Tape Transport</u> Continuous, Read/Write Operations 25 ips, 556 bpi	\$ 9,400
7-608	<u>7 Track Tape Transport</u> Continuous, Read/Write Operations 25 ips, 800 bpi	9,400
7-609	<u>9 Track Tape Transport</u> , continuous Read/Write operations, 25 ips, 800 bpi	9,900
7-610	<u>Optional Hardware Cyclic Redundancy Check</u> provides complete IBM compatibility by hardware generation of CRC character (requires 7-609).	750
	Magnetic Drum Storage Magnetic Drum Storage System includes power supply and necessary mounting hardware. (requires 7-201 and 7-203). Average transfer rate 230 KC; Average access time 8.7 milliseconds (17.4 milliseconds for 7-731).	
7-725	<u>131 KB Storage</u> 117 VAC, 1 ϕ , 60 Hz	16,500
7-726	<u>262 KB Storage</u> 117 VAC, 1 ϕ , 60 Hz	18,500
7-727	<u>524 KB Storage</u> 117 VAC, 1 ϕ , 60 Hz	21,500
7-728	<u>1,048 KB Storage</u> 117 VAC, 1 ϕ , 60 Hz	31,500
7-729	<u>2,096 KB Storage</u> 117 VAC, 1 ϕ , 60 Hz	42,000
7-730	<u>4,192 KB Storage</u> 208 VAC, 3 ϕ , 60 Hz	72,900
7-731	<u>8,384 KB Storage</u> 208 VAC, 3 ϕ , 60 Hz	79,900
7-733	<u>50 Hz option</u> (all 117 VAC system require 220 VAC at 50 Hz and all 208 VAC system require 380 VAC at 50 Hz)	N/C
	SYSTEM MODULES	
7-810	<u>Interrupt Line Module</u> 8 program controlled priority interrupts with arm/disarm, mask/unmask capability.	1,400
7-811	<u>Byte Input/Output Module</u> 8 stored data output lines, 8 data input lines, 8 control lines, 8 sense lines, 1 priority interrupt line.	1,400

PRODUCT NUMBER	DESCRIPTION	UNIT PRICE
	SYSTEM MODULES (Cont.)	
7-812	<u>Halfword Input/Output Module</u> 16 stored data output lines, 16 data input lines, 8 control lines, 8 sense lines, 1 priority interrupt line.	\$ 1,600
7-820	<u>Control Line Module</u> 16 buffered control lines for activation of up to 16 external drives.	1,000
7-821	<u>Relay Closure Module</u> 16 isolated reed relay closures with storage registers for operation of medium power external devices.	1,200
7-822	<u>Decimal Indicator Module</u> 4 decades of decimal indicators	1,900
7-823	<u>Decimal Indicator Module</u> 8 decades of decimal indicators	2,600
7-824	<u>Decimal Indicator Module</u> 4 decades of decimal indicators with decimal point	2,000
7-825	<u>Decimal Indicator Module</u> 8 decades of decimal indicators with decimal point	2,700
7-830	<u>Sense Line Module</u> 16 sense lines which may be used for detecting the status of devices under external command.	1,000
7-831	<u>Sense Switch Module</u> 16 switches for manual entry of program variables	1,200
7-832	<u>Manual Data Entry Module</u> 8 decades of thumb-wheel switches and a 'Data Entry' push button.	1,500
7-833	<u>Manual Data Entry Module</u> 16 decades of thumb-wheel switches and a 'Data Entry' push button.	1,800
7-834	<u>General Purpose Interface Module</u> Basic Input/Output Interface without buffering	700
7-835	<u>Digital Voltmeter Interface</u> Fully buffered interface to the Dana DVM Model 5403 63, 64, or 65-D2 Digital Input/Output Multiplexor Equipment	1,300
7-870	<u>Digital Multiplexor Controller</u> Universal interface for both input and output scanner modules. Only one of these cards is required for system of up to 1,024 lines.	1,200
7-871	<u>Digital Multiplexor Controller</u> with a 60 Hz Clock Same as 7-870 plus 60 cycle	1,500

PRODUCT NUMBER	DESCRIPTION	UNIT PRICE
	SYSTEM MODULES (Cont.) clock which generates interrupts at 16-2/3 milli- second intervals.	
7-873	<u>64 Line Input Scanner Module</u> (Requires 7-870 or 7-871)	\$ 900
7-874	<u>64 Line Output Control Module</u> (Requires 7-870 or 7-871)	1,100
7-875	<u>64 Line Cable</u> Connects the multiplexed lines from the 7-873 or 7-874 modules to cinch connectors for easy access.	250
	Digital Clocks	
7-890	<u>60 Cycle Clock</u> Provides a real time programmable interrupt every 25 or 250 milliseconds	800
7-891	<u>Precision Real Time Clock</u> Provides a real time program interrupt at 1 millisecond, 10 millisecond, 100 milli- second and 1 second intervals.	1,000
7-892	<u>Variable Interval Precision Clock</u> Provides a real time programmable interrupt at variable intervals from 100 microseconds to 2.55 seconds.	1,300
	INTERFACE EQUIPMENT	
	Character Buffered Half Duplex Line Adapters	
10-023	<u>Bell 103 Data Set Adapter</u>	1,600
10-024	<u>Bell 201 Data Set Adapter</u>	1,500
10-025	<u>Bell 202 Data Set Adapter</u>	1,600
10-027	<u>Parity Option for 10-023/24/25</u>	100
	Host Computer Interfaces	
11-004	<u>Universal INTERDATA to IBM 360 Interface</u>	8,100
11-010	<u>INTERDATA to B5500</u>	7,100
11-020	<u>INTERDATA to Univac 1108</u>	9,800
	CONVERSION EQUIPMENT	
	Multichannel Analog to Digital Converters Provides fully interfaced conversion of bipolar analog signals; and can multiplex up to 64 analog channels in both random or sequential selection modes.	
7-751	<u>A-D Converter with buffering</u> 8 bit	1,900
7-752	<u>A-D Converter with buffering</u> 10 bit	2,100
7-753	<u>A-D Converter with buffering</u> 12 bit	2,400

PRODUCT NUMBER	DESCRIPTION	UNIT PRICE
	CONVERSION EQUIPMENT (Cont.)	
7-754	<u>Sample and Hold Amplifier</u> (Maximum of 1 per 64 channels)	\$ 500
7-771	<u>4 Channel Multiplexor</u> (Requires 7-751, 7-752, 7-753)	500
7-772	<u>8 Channel Multiplexor</u> (Requires 7-751, 7-752, 7-753)	600
7-773	<u>12 Channel Multiplexor</u> (Requires 7-751, 7-752, 7-753)	700
7-774	<u>16 Channel Multiplexor</u> (Requires 7-751, 7-752, 7-753) Maximum of 4 Multiplexor Boards per System	800
	Multichannel Digital to Analog Converters Provides fully interfaced conversion of digital signals to bipolar analog signals. The system can address up to 16 channels in random or sequential modes. Each channel employs dual rank registers and an operational amplifier.	
7-764	<u>D-A Controller for up to 16 channels.</u> (Requires 7-761, 7-762, 7-763)	800
7-761	<u>Dual Channel D-A Converter</u> 8 bit	1,200
7-762	<u>Dual Channel D-A Converter</u> 10 bit	1,300
7-763	<u>Dual Channel D-A Converter</u> 12 bit	1,600
	EXPANSION CHASSIS	
7-990	<u>System Chassis</u> Prewired to handle up to 8 KB memory expansion plus 10 controller cards.	900
7-991	<u>System Chassis</u> Prewired to handle up to 24KB memory expansion plus 5 controller cards.	1,100
7-992	<u>System Chassis</u> Prewired to handle up to 40KB memory expansion. No controller card availability.	1,200
7-993	<u>System Chassis</u> Prewired to handle up to 13 controller cards only	1,000
7-985	<u>Power Supply Expansion</u> Provides normal power for two additional expansion chassis.	800

PRODUCT NUMBER	DESCRIPTION	UNIT PRICE
7-980	ENCLOSURES <u>Desk Top Cabinet for Model 3 or 4</u> Houses processor and power supply, provides for display panel mounting; contains fan assembly.	\$ 300
7-989	<u>System Cabinet</u> Houses processor with power supply and four system chassis, can mount general purpose display, paper tape reader and punch, or other RETMA rack mounting equipment; with front and rear doors, shelf and fan assembly.	1,000
3-992	TEST EQUIPMENT X-Ray ROM A plug-in Read-Only-Memory which replaces the normal ROM during maintenance. <u>X-Ray ROM for Model 3</u>	1,200
4-992	<u>X-Ray ROM for Model 4</u> System Test Set Displays pertinent registers and buses, contains an adjustable clock and memory threshold adjustment.	1,500
3-993	<u>System Test Set Model 3</u>	1,500
4-993	<u>System Test Set Model 4</u>	1,500

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Practically prodigious is the Interdata family of computers now available with our unique Mass Core Memory. *It's Practical:* For the first time low cost Mass Memory is available with a powerful 3rd generation computer for those jobs requiring large core resident programs. This offers you greater reliabil-

ity and operating simplicity than any comparable peripheral storage unit. *It's Prodigious:* Teamed with an Interdata General Purpose or Communications Processor you have 65K *directly addressable* bytes of memory, over 75 standard instructions, 16 general registers, a host of options and lots of Firm-

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The Model 4

A total approach
to General Purpose
Computing

 **INTERDATA®**



THE MODEL 4 — A TOTAL APPROACH TO GENERAL PURPOSE COMPUTING

Introduction to the Model 4

The INTERDATA Model 4 is a significant departure from the conventional structure of the small computer. The Model 4 represents the latest advances in 3rd generation concepts to provide you with the powerful features of larger computers, at small computer prices.

Features like:

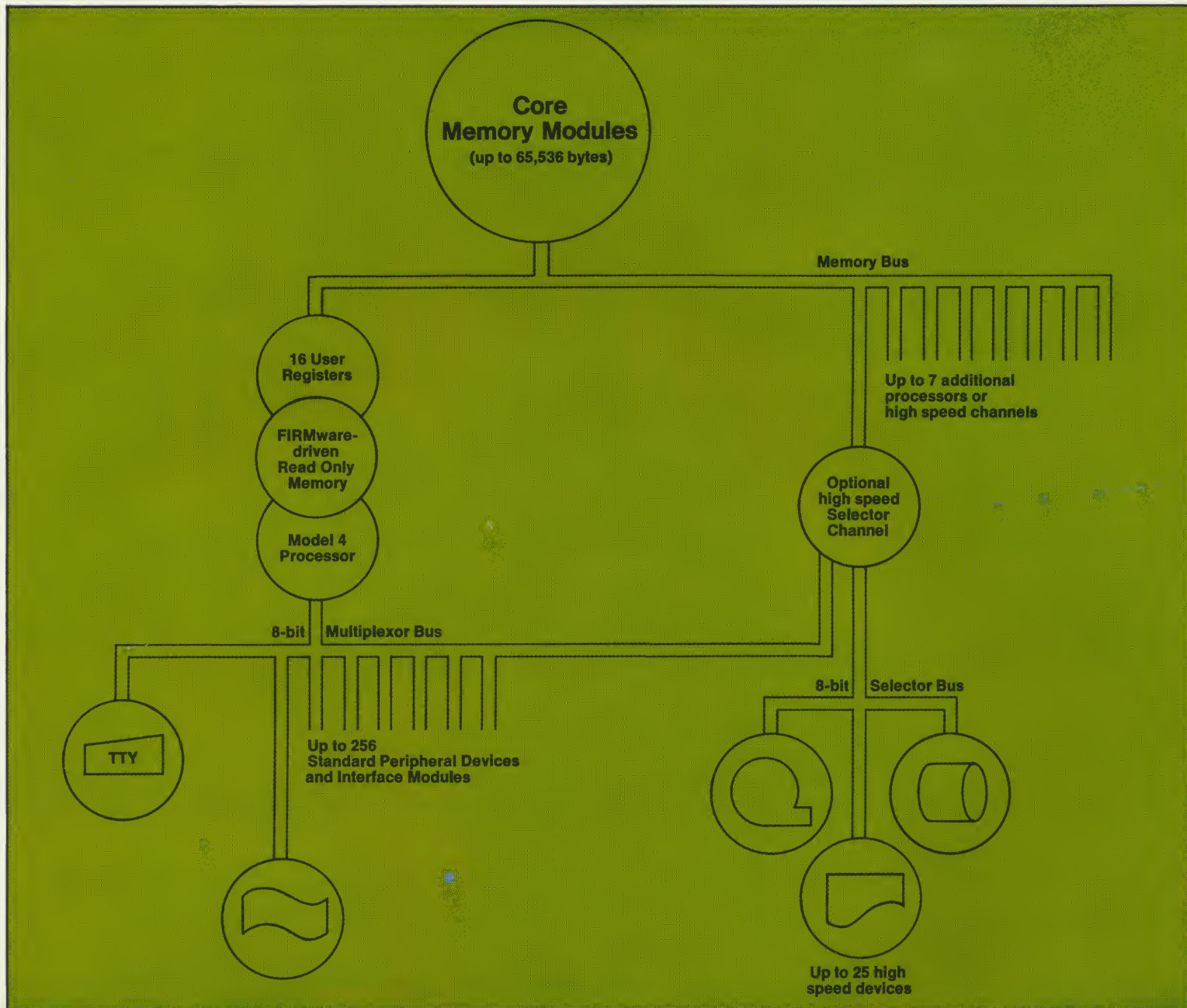
- 16 hardware general registers
- 1 microsecond core memory cycle time
- up to 65K bytes of memory — directly addressable
- 75 basic instructions
- 15 hardware index registers.
- extensive software library
- a sophisticated I/O structure
- a complete line of peripherals

Feature	Typical 2nd Gen. Computers	3rd Gen. Computer
Register	1 accumulator 1 index register	16 accumulators, 15 of these can be as index registers
Instruction Sets	small — often only 8-16 basic	75 basic instructions
Instructions Options	limited usually to multiply/divide	expandable through FIRMware
Addressing	limited capacity requires "paging" or "sectorizing"	direct addressing of up to 65,536 bytes eliminates paging
Word length	Fixed	multiple: 8, 16 and 32 bit
I/O Structure	uses software "polling techniques"	Automatic hardware interrupting device identification and status monitoring

Architecture

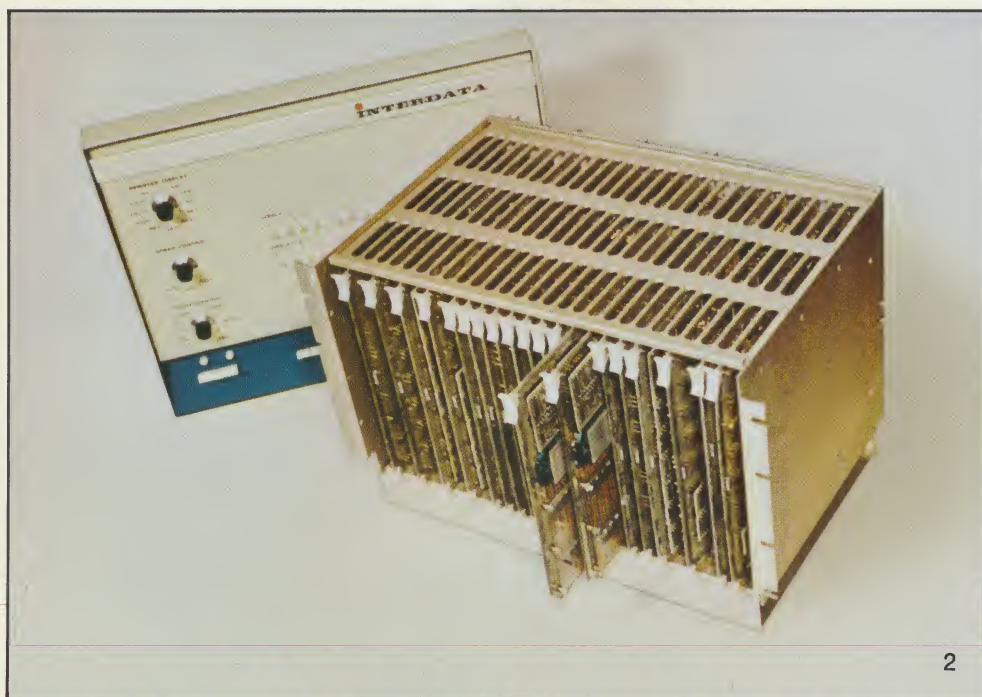
The INTERDATA Model 4 is modularly structured to provide a high degree of flexibility in configuring application-oriented systems. Up to 8 processors, High

Speed Memory Bus Interfaces, or Selector Channels may be connected to the Memory Bus. Memory is field expandable to 65K bytes — requiring only plug-in of additional modules to a pre-wired chassis.



Interdata digital systems are modularly structured to provide a high degree of flexibility in configuring application-oriented systems. The "building blocks" are all expandable to allow the system to grow with its user's needs. A combination of up to 8 processors, Selector Channels or Direct Memory Access Channels may be connected to the Memory Bus. Field Expansion of memory requires only plug-in of additional modules to a pre-wired chassis. The memory modules of most Interdata systems can be expanded to a maximum direct addressing range of 65,536 bytes.

Shown at right is a basic Model 4 central processor with 8K bytes of memory and I/O slots for three peripheral devices.



FIRMware

The FIRMware concept, pioneered by INTERDATA, is a technique whereby a microcoded "inner processor" functions as the control mechanism of the main computer. Operating at 400 nanoseconds per cycle, FIRMware directs register manipulations and data transfers within the computer.

The FIRMware program is hardwired into a permanent nondestructible read-only-memory (ROM), resulting in a highly versatile machine which offers an impressive price performance ratio.

FIRMware Support INTERDATA provides the Model 4 with software packages allowing the user to assemble and simulate his microcoded program very much the same as a software program.

FIRMware Assemblers These programs accept source tapes for micro-programs and generate ROM object tapes. With these assemblers, micro-operation codes have symbolic names, operands have symbolic names, numbers can be written in a natural way, locations have symbolic names, and error checking is performed. These assemblers run on any standard INTERDATA system with 8K bytes of memory and a teletype.

Simulators The simulators are used for testing and debugging micro-programs before they are wired into a ROM. The simulators

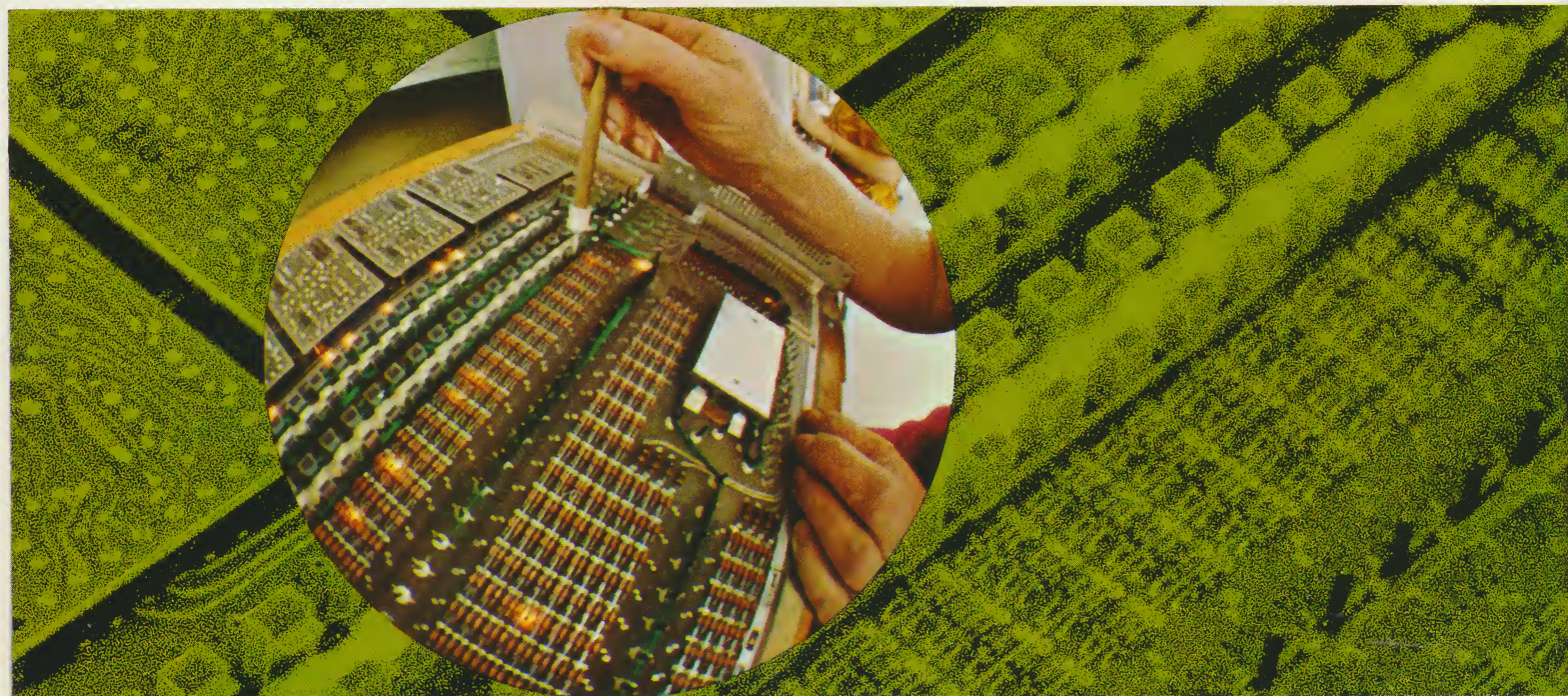
are interactive and allow the debugging process to proceed under teletype control with continuous observation by the designer. The simulators will read ROM object tapes, execute the micro-programs, and punch a corrected ROM object tape. 8k bytes of memory are required.

The result is a customized computer tailored to the individual users needs, while preserving the software features of a general purpose machine.

FIRMware Options The versatility and programming power of the Model 4 is further enhanced by a wide array of application oriented FIRMware optional packages. These packages are offered as plug-in or replacement read-only-memory modules. Field expansion is possible in most instances.

FIRMWARE packages available are:

1. High Speed Option
2. Fullword Instruction Set
3. Floating Point Expansion
4. Floating Point Trigonometric Expansion
5. Text Editing
6. Memory Accumulator Instruction Set
7. Indirect Instruction Set
8. Push down Table Manipulating Set



Software

INTERDATA's library of software packages has been designed to take advantage of the programming ease and power of the Model 4. This library includes: Fortran IV, Assembler, Real-Time Executive, On-line interactive debugging, Text Editor, extensive math library and I/O systems packages.

Fortran IV The Fortran IV Compiler for INTERDATA Digital Systems allows users to generate machine language programs using a problem-oriented language. The Fortran language is USASI Fortran IV, tailored to the real-time environment. Language features for manipulating interrupts and handling real-time input/output are provided. Assembly language statements and Fortran statements can be intermixed. The compiler provides extensive diagnostics during compilation to assist the user. The Fortran compiler requires 16K bytes of memory and operates under the INTERDATA Executive Systems. The generated object code is relocatable.

Program Preparation on Other Computers INTERDATA customers have access to assemblers and compilers which operate on larger general purpose computers or on time sharing networks. A basic assembler, written in Fortran IV, and

an expanded assembler, written in PL1, are available. An assembler and simulator for INTERDATA systems are currently running on several time sharing systems.

Executive — The Basic Executive is designated to operate on a Model 4 with 8K bytes of core memory plus one teletype for operator communication and user I/O. The system loads and initiates program execution under operator control. It performs logical I/O for all standard peripherals — Teletype, Card Reader, Magnetic Tape, etc. I/O handlers are modular and can be included as required by each installation. The basic executive expands to include the capability of loading and executing programs from libraries residing on mass storage devices.

The Real-Time Executive, which requires 16K bytes, a real-time clock, and memory protect, provides all of the capabilities of a basic executive. It adds ability of scheduling the execution of programs based on a real-time clock and real-time events. The system handles re-entrant real-time foreground programs plus background processing. The addition of mass storage enables the system to handle nonresident foreground programs.

Debugging An on-line interactive program allows examination and

modification of core memory in hexadecimal notation. Bias handling is provided for referencing and displaying relocatable programs. Object tapes can be generated for any block of memory in either 8-bit or standard binary tape formats. Symbolic disassembly of programs from core memory is provided.

Features available to the user are:

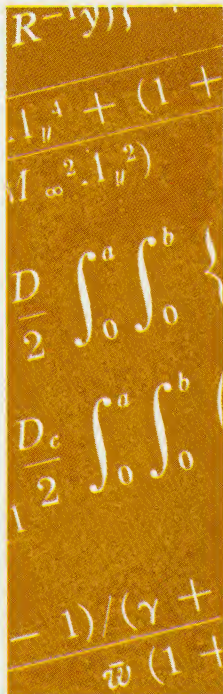
- Examine and modify a memory cell
- Address arithmetic
- Relative addressing of memory
- Multiple break points
- Search on limits for masked value
- Print or punch content of memory
- Execute the user programs
- Register examination

Editor An on-line interactive text editor allows direct entry of source statements into memory. These statements can be freely listed, changed, deleted, or augmented while remaining in core memory. Edited statements can then be output to form a source tape.

Math Library A complete math library of function routines in fixed and floating point is provided with INTERDATA systems.

Input/Output The input/output system provides driver packages for peripheral devices and system modules in addition to media conversion utility routines.

Model 3 and Model 4 multiprocessor systems for a multi-task control application.



Instruction Repertoire

A simple instruction repertoire may mean months of struggling for your programmers . . . a powerful instruction repertoire will not only make their task much easier but, combined with multiple registers, and other 3rd generation features, will dramatically improve the real time performance of the system.

What comprises a powerful instruction repertoire? One manufacturer lists 75 instructions when, in effect, his processor provides only 8 basic functions. Many of the others use the same tactics by listing dozens of trivial combinations.

The INTERDATA instruction set has 55-57 basic instructions plus options. They operate at highly effective speeds due to 3rd generation architecture; they are purposely designed for real time scientific and industrial applications.

Third Generation Instruction Format

Register to Register format: RR

0	7	8	11	12	15
OP	R1		R2		

Register to Indexed Memory format: RX

0	7	8	11	12	15	16	31
OP	R1		X2	Address			

Register to Indexed Data format: RS

0	7	8	11	12	15	16	31
OP	R1		X2	Data			

Program Status Word

0	11	12	15	16	31
Status	Condition Code		Instruction Address		

The system has three instruction formats. The 16-bit halfword instructions are the RR format. The 32-bit fullword instructions are the RX and RS formats.

The 4-bit R1, R2 (and X2) fields each specify one of the sixteen general registers. Each of the 16 halfword general registers can be used as a fixed point arithmetic accumulator or as a logical accumulator. Fifteen of the 16 general registers can be used as index registers.

The RR instructions are for operations between the general registers. The R1 and R2 fields specify the first and second operands respectively. For a register-to-register Add operation $[(R1) + (R2) \rightarrow (R1)]$.

The RX instructions are for operations between the general registers and memory. The R1 field specifies the first operand and the sum of the X2 and Address field specify the address of the second operand. For a register-to-indexed memory Add operation $[(R1) + (Address + X2) \rightarrow (R1)]$.

Immediate instructions RS are included for shifting and branching. Operations involving immediate operands also use the RX format. For the immediate instruction the R1 field specifies the first operand and the sum of the contents of the X2 and Address field form the second operand. For an Add immediate operation $[(R1) + Address + (X2) \rightarrow (R1)]$. The shift count is given by $[Address + (X2)]$.

Instruction alignment — Halfword RR format instructions and fullword RX and RS format instructions are aligned on halfword boundaries. This permits mixing of halfword and fullword instructions with no requirement for halfword NO-OP's to force correct fullword instruction memory alignment.

Program Status Word — The status of the machine is defined by the program status word. It contains the Status, Condition Code and Instruction Address.



Instruction Repertoire

Type	Instruction	Mnemonic
Load and Store Instructions	Load Halfword	LHR
	Load Halfword	LH
	Load Halfword immediate	LHI
	Store Halfword	STH
	Load Byte	LBR
		LB
	Store Byte	STBR
		STB
	Load Program Status Word	LPSW
	Unchain	UNCH
Fixed Point Arithmetic Instructions	Load Multiple	LM
	Store Multiple	STM
	Autoload	AL
	Add	AHR
		AH
		AHI
	Add with Carry Halfword	ACHR
		ACH
	Subtract Halfword	SHR
		SH
Logical Instructions		SHI
	Subtract with Carry Halfword	SCHR
		SCH
	AND Halfword	NHR
		NH
		NHI
	Inclusive OR Halfword	OHR
		OH
		OHI
	Exclusive OR Halfword	XHR
Input output Instructions		XH
		XHI
	Compare Logical Halfword	CLHR
		CLH
		CLHI
	Read Data	RDR
		RD
	Write Data	WDR
		WD
	*Read Block (optional)	RBR
Device Interrupt Control Instructions		RB
	*Write Block (optional)	WBR
		WB
	Acknowledge Interrupt	AIR
		AI
	Sense Status	SSR
		SS
	Output Command	OCR
		OC
	Shift Left Arithmetic	SLHA
Shift Instructions	Shift Right Arithmetic	SRHA
	Shift Left Logical	SLHL
	Shift Right Logical	SRHL
	Branch AND Link	BALR
		BAL
	Branch on False Condition	BFCR
		BFC
	Branch on True Condition	BTCR
		BTC
	Branch on Index Low or Equal	BXLE
Branch Instructions	Branch on Index High	BXH
	Branch Unconditional	BR
		B
	Branch on Zero	BZ
	Branch on Not Zero	BNZ
	Branch on Plus	BP
	Branch on Not Plus	BNP
	Branch on Minus	BM
Extended Mnemonics		

Type	Instruction	Mnemonic
	Branch on Not Minus	BNM
	Branch on Carry	BC
	Branch on Overflow	BO
	Branch on Low	BL
	Branch on Not Low	BNL
	Branch on Equal	BE
	Branch on Not Equal	BNE
	No Operation	NOPH
		NOP
STANDARD OPTIONS		
Fixed Point Arithmetic Instructions	Multiply Halfword (optional)	MHR
		MH
	Divide Halfword (optional)	DHR
		DH
	Floating Point Arithmetic Instructions (optional)	AE
	Add	SE
	Subtract	ME
	Multiply	DE
	Divide	LE
	Load	STE
Floating Point Trigonometric Instructions	Store	CE
	Compare	
	Floating Point Square Root (RR)	SQER
	Floating Point Square Root	SQE
	Floating Point Sine	SINE
	Floating Point Cosine	COSE
	Floating Point Arc Tangent	ACTE
	Load Fullword	L
	Store Fullword	ST
	Add Fullword	A
Fullword (32 bit) Fixed Point Instructions	Subtract Fullword	S
	Compare Fullword	C
	Shift Left Fullword Logical	SLL
	Shift Right Fullword Logical	SRL
	Rotate Left Fullword	RL
	Rotate Right Fullword	RR
	Compare Logical Byte (RR)	CLBR
	Compare Logical Byte	CLB
	Translate (RR)	TRNR
	Translate	TRN
Text Editing Instructions	Move (RR)	MOVR
	Move	MOV
	Find (RR)	FNDR
	Find	FND
	Load Indirect	LI
	Store Indirect	STI
	Branch on True Condition Indirect	BTCI
	Branch on False Condition Indirect	BFCI
	Branch AND Link Indirect	BALI
	Add Halfword to Storage	AHS
Advanced Programming Package Instructions	Subtract Halfword to Storage	SHS
	AND Halfword to Storage	NHS
	Inclusive OR Halfword to Storage	OHS
	Exclusive OR Halfword to Storage	XHS
	Push	PHS
	Pop	POP
	Chain	CHN
	Unchain	UNCH
	Branch IF Multiplexor	BIM
	Execute IF Multiplexor	EIR
Special Instructions	Test Bit	TB
	Set Bit	SB
	Clear Bit	CB

* Optional Firmware Instructions

I/O Structure

An I/O Structure which "unjams" the accumulator

In most small computers, information coming from and going to the outside world passes through a single accumulator. This continuously requires instructions to unload and reload the previous computation. Not so with the INTERDATA Model 4. In the Model 4 structure, I/O transforms can be deposited in a spare accumulator within the 16 register stack WITHOUT affecting the previous computation. In addition, the data can be placed directly into memory — either under program control or over the optional cycle stealing ports such as the Selector Channel.

Automatic Hardware Polling with Simultaneous Device Status

Many small computers require a considerable quantity of software processing to successfully interrogate devices to determine the interrupt source. The Model 4 structure embeds these housekeeping functions in hardware. The result is greater utilization of critical processor time.

I/O Control Concept The Model 4 I/O structure employs a highly reliable I/O request-response control mechanism. It is an automatic function which avoids "tricky" synchronization. This form of request-response takes no appreciable time and provides locked-in insurance against timing errors due to possible component degradation or environmental noise. As a result, interfacing problems are greatly simplified.

FIRMWARE enhances I/O Functions

Special purpose FIRMWARE can be employed to further enhance real time I/O processing. At 400 nanosecond cycle speeds, FIRMWARE can perform extensive I/O control and data management. The resulting improvement in throughput can be from 3 to 10 times when compared to the performance of the same functions through software.

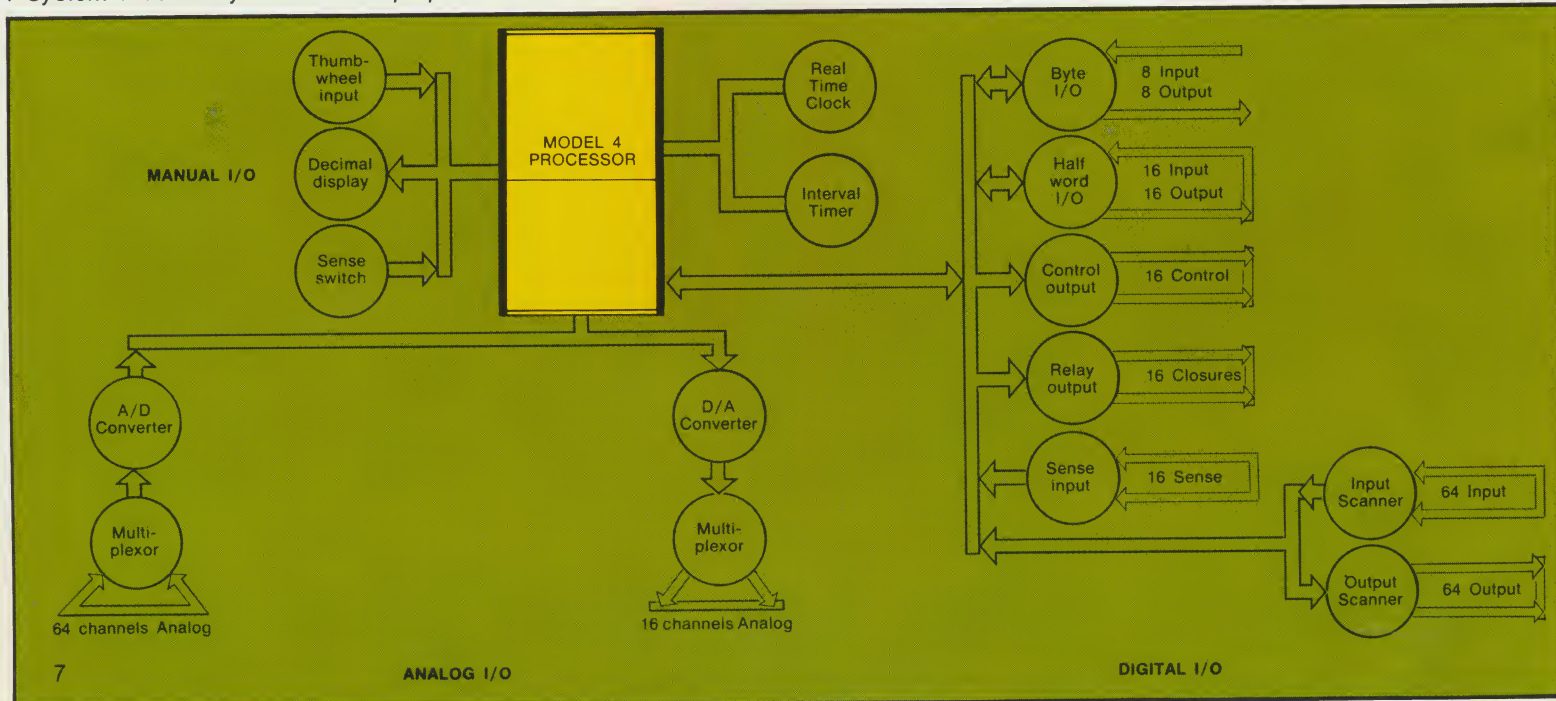
I/O Channels The 8-bit Model 4 Multiplexor Channel transfers byte oriented data under program control

between the processor and an active device. Either single bytes or a block of bytes can be transferred depending on the instruction used. Under program interrupt control a number of low speed devices can be operational at the same time. The interrupt organization permits the individual unique identification of up to 256 devices in a hardware priority structure with overriding enable/disable facilities. An optional 8-bit Selector Channel provides high speed, byte oriented data transfer between memory and an active device. The Selector Channel is initialized for block transfer by the processor, thereby freeing the processor for other work.

Standard Memory Bus Interface

The Standard Memory Bus Interface permits the user access to a 16 bit data word on a cycle stealing basis. This is provided as an optional system module for interfacing with customers special I/O devices.

System Modules to meet virtually all requirements. The success of a real-time system is based upon the efficiency of the Model 4 System Modularity. This concept permits the Model 4 to handle diverse analog and digital interface problems at minimal cost.



Peripheral Equipment

An outstanding line of field-proven peripheral equipment is available for the Model 4 system. These peripherals are designed to handle a wide range of user processing tasks.

The following peripheral equipment is available for the Model 4:

Teletype

ASR 33 — Available with a 10 cps read/punch/type speed
KSR 33, KSR 35, ASR 35 — Heavy duty types which complement the ASR 33 and the new ASR 37
GE Termi-Net 300 — Useful for higher speed applications

Paper Tape Equipment

A 300 cps reader and 60 cps punch are offered for the Model 4, individually, or as a complete package. Fan-fold tape is featured as the software media.

Card Reader

A 200 cpm reader is provided for card oriented input systems

Line Printer

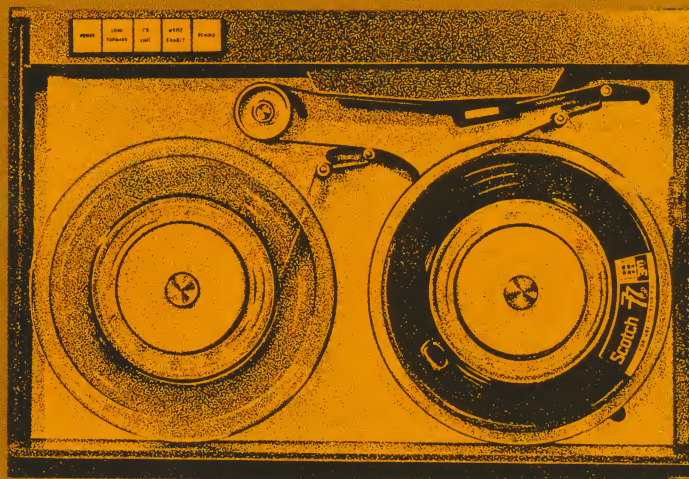
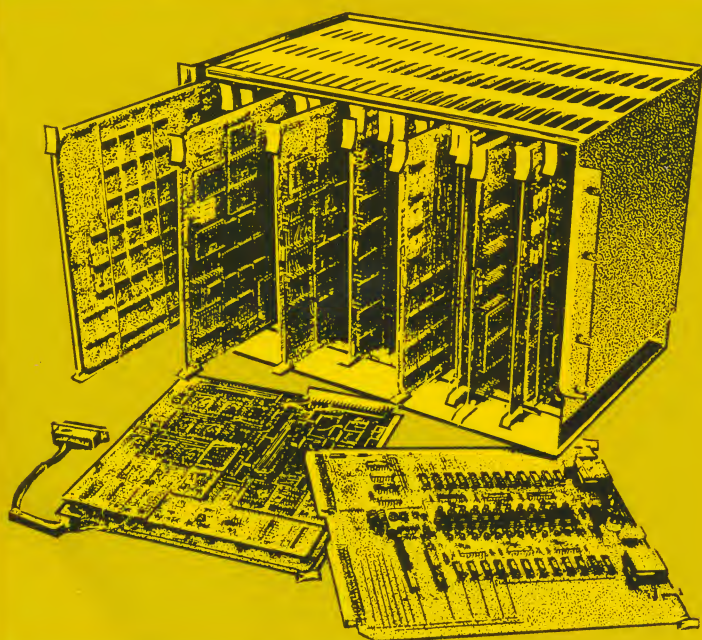
Provides 300 lpm capability with 132 columns per line and 64 characters. Ideally suited to fulfill your high speed listing requirements.

Bulk Storage

Fast access bulk storage media is offered in 131KB to 8.3MB sizes. Average transfer rates are 230KB/second with 8.7 and 17.4 microsecond average access times. IBM compatible seven and nine track tape transports are available for the Model 4 with 25 ips speed and densities of 556 bpi and 800 bpi.

Communication Devices

Line adapters for a broad spectrum of communication requirements are offered. Host computer interfaces for the IBM/360, Univac 1108, and Burroughs 5500 are also available for the Model 4. Data set adapters for Bell units include the 103, 201, 202, and 301 with various options.



Customer Support

With hundreds of installed computer systems, INTERDATA maintains an extensive program of customer support activities. You are encouraged to avail yourself of these services in order to effectively utilize the Model 4's capabilities.

Customer Training Hundreds of customers attend INTERDATA's year-round training school. Additional training is provided on-site where requested. Courses pertinent to the Model 4 include: Software and Hardware instruction, FIRMWARE instruction, and a special course in maintenance.

Field Service Qualified factory trained personnel are at your disposal 24 hours a day should you experience difficulty with your Model 4, and they are as close as your nearest INTERDATA sales office.

Application Support For the many customers who require special support, INTERDATA offers a senior team of hardware, software, and FIRMWARE specialists whose background includes data acquisition systems, testing systems, process control systems, and data com-

munications. INTERDATA's sales engineers have long experience with small computer applications. They can give you valuable local assistance in planning and dimensioning your application.

Quality Control Quality Control at INTERDATA begins with detailed mechanical and electrical inspection of all components utilized in manufacturing a Model 4. Each stage

of assembly is carefully monitored through the employment of automatic and semi-automatic test equipment. Logic boards, for example, are checked with our own computers. In addition, ALL computers are given extensive environmental chamber evaluation prior to shipment. This total approach to Quality Control insures quick, trouble-free installation and a high degree of reliability.



Model 4

Basic Specifications

Data Word Length — 8, 16, 32 bits
(parity option)

Memory Cycle Time —
1.0 microsecond — Core Memory
400 nanosecond — Read-only-memory

Word Size — 16 bits

General Registers — 16 hardware
registers (16 bits each)

Hardware Index Registers — 15 general
registers may be used for indexing

Basic Memory — 4K bytes, expandable
to 65K bytes

Directly Addressable Memory — 65K bytes

Machine Code — Two's Complement

Instruction Repertoire — over 75 standard
instructions

16 bit—Load Halfword—2.8 microseconds

16 bit—Add Halfword—3.2 microseconds

16 bit—Multiply—3.8 microseconds
(optional)

Input/Output

Program Transfer — 25KBS

Block Transfer — 150 KBS (with high
speed option 4-101)
500 KBS (with selector
channel 7-201)

Interrupts — 2-256 levels
8 levels with arm/disarm
and mask (optional)

Display Panel

Control Switches — Power initialize
execute

Mode Control — Run, halt, single op,
variable speed, address input, memory
location, memory data

Speed Control — Variable, 1 cycle/sec
to 100 cycle/sec

Display — Two registers simultaneously
selectable

Switches — Sixteen data/sense

Mechanical

Size — 10½" x 19" x 4" (rack
mountable)

Power — 325 watts, 115 VAC ± 10%,
47-63 hertz

Weight — 56 lbs.

Temperature:

Operating — 0° to 50°C

Storage — 55° to 85°C

Humidity — 0 to 90% relative

Reliability

MTBF — 6,000 hrs. (Mainframe and
4KB Memory)

I would like additional information on the Model 4. Please have a sales engineer phone me at _____

NAME _____

STREET _____

CITY _____

STATE _____

ZIP CODE _____

My application is _____

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Suite 305
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Dear Sir:

Thank you for your recent inquiry. I believe you will find the enclosed literature interesting and of significant value to you.

As a potential INTERDATA customer, you should know that we have installed over 300 computer systems in a wide variety of general purpose and communication environments - a testimony to INTERDATA integrity, customer satisfaction and engineering design capability.

We would be pleased to discuss any facet of our product line with you. Just call your nearest INTERDATA regional office or return the enclosed reply card to our Home Office. Better yet, phone me collect at (201) 229-4040.

Very truly yours,

Daniel Foltz
General Purpose Computers
Technical Support



INTERDATA®

2 CRESCENT PLACE, OCEANPORT, NEW JERSEY 07757

COMPUTER DESIGN

T NELSON, SYS CONSLT

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